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EXAMINER	
MONDT, JOHANNES P	

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2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,633	KOLDIAEV ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/20/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the Information Disclosure Statement filed 08/20/2003; a signed copy of Form PTO-892 is herewith enclosed.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1-20*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al (US 2002/0146879 A1) in view of Gardner et al (6,323,519 B1) and Wolf (ISBN: 0-961672-4-5).

On claim 1: Both the third and second embodiments by Fu et al shall be discussed in this order, while in the sequel, unless expressly stated dependency relies upon the third embodiment:

(A) Third embodiment: Fu et al teach a dielectric spacer structure (third embodiment, Figures 13-16, title, abstract and sections [0067]-[0068]), comprising:

a first oxide layer 504 deposited over a top surface of a wafer 500 and abutting a gate structure 501/502/503 (see section [0067] and Figure 13 for "abutting");

a silicon-nitride barrier layer 505 (section [0067]) deposited over said first oxide layer.

Fu et al do not necessarily teach the further limitations (a)

that said silicon nitride barrier layer be formed without exposing said first oxide layer to a chemical component that nitridizes SiO_2 and Si-SiO_2 interfaces, thereby enabling formation of said silicon nitride barrier layer without nitridizing said first oxide layer; *and (b)* that a second oxide layer be formed over said silicon nitride layer.

The further limitation ad (a) only limits the dielectric spacer structure, rather than the method of making the dielectric spacer structure, through the claimed absence of nitridization of the silicon oxide layer 504 and the interface between said silicon oxide layer 504 and the wafer 500 (formation of said silicon nitride barrier layer without nitridizing said first oxide layer'): the remainder of said further limitation ad (a), i.e., "wherein said silicon nitride layer is formed without exposing said first oxide layer to a chemical component that nitridizes SiO_2 and Si-SiO_2 interfaces", only limits the method of making said dielectric spacer structure. In reference to the claim language referring to ["wherein said silicon nitride layer is formed without exposing said first oxide layer to a chemical component that nitridizes SiO_2 and Si-SiO_2 interfaces"] intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

With regard to the only structural relevant portion of the further limitation ad (a) as defined above, it would have been obvious to include said further structurally relevant portion of further limitation ad (a) in view of Gardner et al, who teach in a patent

on spacer silicon oxide / silicon nitride spacers on gate structures with LDD (see title, abstract and column 1, l. 8-39) a gate structure with a silicon oxide layer underneath a silicon nitride layer 24 (N.B.: 'nitrided oxide' is a narrower term of 'nitride') that is substantially free of nitrogen (col. 4, l. 15-28, Figure 12 and col. 10, l. 9-30) for the specific purpose of lowering the dielectric constant (=permittivity) of the spacer so as to reduce the effects of fringing field and parasitic capacitance between gate and source/drain regions (col. 4, l. 19-28). *Motivation* to include the teaching by Gardner et al in the invention by Fu et al thus derives from reducing the parasitic capacitance.

With regard to the further limitation ad (b) as defined above, it would have been obvious to include said further limitation ad (b) in view of Wolf who teaches the need to apply interlayer dielectric for planarization of gate/source/drain structures for the specific purpose to avoid unwanted steps in the topographic layout, CVD SiO2 being one of the simplest ways to implement said planarization (see sections 4.4.2.2, p. 208 and 4.4.3, p. 221). *Motivation* to include the teaching by Wolf in the invention by Fu flows at least from the avoidance of poor step coverage of metal lines (cf. Wolf, p. 201) that need to reach the source/drain regions such as 510 ([0067]) in Fu et al (Figure 16).

(B) Second embodiment: Fu et al teach a dielectric spacer structure (second embodiment, Figures 9-12, title, abstract and sections [0065]-[0066]), comprising:

a first oxide layer 404 deposited over a top surface of a wafer 400 and abutting a gate structure 401/402/403 (see section [0065] and Figure 9 for "abutting");

a silicon-nitride barrier layer 405 (section [0065]) deposited over said first oxide layer.

Fu et al do not necessarily teach the further limitations (a)

that said silicon nitride barrier layer be formed without exposing said first oxide layer to a chemical component that nitridizes SiO_2 and Si-SiO_2 interfaces, thereby enabling formation of said silicon nitride barrier layer without nitridizing said first oxide layer; *and (b)* that a second oxide layer be formed over said silicon nitride layer.

The further limitation ad (a) only limits the dielectric spacer structure, rather than the method of making the dielectric spacer structure, through the claimed absence of nitridization of the silicon oxide layer 404 and the interface between said silicon oxide layer 404 and the wafer 400 (formation of said silicon nitride barrier layer without nitridizing said first oxide layer'): the remainder of said further limitation ad (a), i.e., "wherein said silicon nitride layer is formed without exposing said first oxide layer to a chemical component that nitridizes SiO_2 and Si-SiO_2 interfaces", only limits the method of making said dielectric spacer structure. In reference to the claim language referring to ["wherein said silicon nitride layer is formed without exposing said first oxide layer to a chemical component that nitridizes SiO_2 and Si-SiO_2 interfaces"] intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

With regard to the only structural relevant portion of the further limitation ad (a) as defined above, it would have been obvious to include said further structurally

relevant portion of further limitation ad (a) in view of Gardner et al, who teach in a patent on spacer silicon oxide / silicon nitride spacers on gate structures with LDD (see title, abstract and column 1, l. 8-39) a gate structure with a silicon oxide layer underneath a silicon nitride layer 24 (N.B.: 'nitrided oxide' is a narrower term of 'nitride') that is substantially free of nitrogen (col. 4, l. 15-28, Figure 12 and col. 10, l. 9-30) for the specific purpose of lowering the dielectric constant (=permittivity) of the spacer so as to reduce the effects of fringing field and parasitic capacitance between gate and source/drain regions (col. 4, l. 19-28). *Motivation* to include the teaching by Gardner et al in the invention by Fu et al thus derives from reducing the parasitic capacitance.

With regard to the further limitation ad (b) as defined above, it would have been obvious to include said further limitation ad (b) in view of Wolf who teaches the need to apply interlayer dielectric for planarization of gate/source/drain structures for the specific purpose to avoid unwanted steps in the topographic layout, CVD SiO2 being one of the simplest ways to implement said planarization (see sections 4.4.2.2, p. 208 and 4.4.3, p. 221). *Motivation* to include the teaching by Wolf in the invention by Fu flows at least from the avoidance of poor step coverage of metal lines (cf. Wolf, p. 201) that need to reach the source/drain regions such as 410 ([0065]) in Fu et al (Figure 12).

On claim 2: the dielectric spacer structure as essentially taught by Fu et al, Gardner et al and Wolf further comprises a second silicon nitride layer 406 ([0066]) in the second embodiment, and 506 ([0068]) in the third embodiment, formed between said silicon nitride barrier layer 405 in the second embodiment, 505 in the third embodiment, and said second oxide layer (as taught by Wolf), while the further

limitations defined by the wordings that said second silicon nitride layer is an "etch stop" layer and "wherein said etch stop nitride layer is formed through a process that includes ammonium precursors" solely constitute limitations on the method of making and not on the structure, as we have seen before through the teaching by Gardner et al that the first oxide layer (and hence also the interface between the first oxide layer) can be made substantially free of nitrogen even without necessarily including said further limitations (col. 4, l. 15-28, col. 8, l. 36-56, col. 10, l. 8-30). Applicant is reminded that it has been held that In reference to the claim language referring to a method of forming or making, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim, and, being entirely identical in constitution as claimed is capable to achieve the same intended use. See: In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

On claim 3: Fu et al at least in their third embodiment teach that atomic layer deposition (ALD) is used for the deposition of the silicon nitride barrier layer. Please note for future reference that ALD is selected so as to improve the hydrogen content in the silicon nitride layer from "reduced" in the LPCVD method of the third embodiment ([0067]) to "substantially absent or without" in the teaching for the third embodiment ([0067]).

On claim 4: Fu et al do not necessarily teach the ALD (atomic layer deposition) method of their third embodiment to be based on nitridizing *by plasma process* for the

formation of the silicon nitride barrier layer. However, Applicant, in the specification, does not disclose any structural features distinguishing the final structure resulting from the application of ALD by nitridizing through a plasma process from the invention as essentially taught by Fu et al, Gardner et al and Wolf (meeting claim 1), because contamination by nitrogen in the underlying first oxide layer is substantially absent according to Gardner et al (col. 4, l. 15-28 and col. 10, l. 12-13), and hence there is no formation of oxynitride (see pages 15 and 16 of the Specification) in said first oxide layer, which appears to be the only structural advantage, as opposed to advantage of fast and economical making (pages 15 and 16 of the Specification).

In reference to the claim language referring to formation by plasma process as delineated above, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See: In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

On claims 5-7: In reference to the claim language referring to formation of said silicon nitride barrier layer through vapor deposition of a nitrogen-silicon gas containing a non-ammonia based organic precursor as defined by claims 5, 6 and 7, intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See: In re Casey, 152 USPQ 235 (CCPA 1967);

In re Otto, 136 USPQ 458, 459 (CCPA 1963). Although Applicant achieves the absence of nitrogen in the underlying first oxide layer by avoiding the use of ammonia, be it through use of organic precursor that does not contain ammonia, or vapor deposition of N_2 and $SiCl_2$, or vapor deposition of N_2 and SiF_4, in the invention as essentially taught by Fu et al, Gardner et al and Wolf said avoidance is achieved either by making the underlying first oxide layer thick enough or by exposing the oxide layer to vapor in a CVD during a short enough time (see Gardner et al, col. 4, l. 15-28). Hence, indeed no structural difference is necessarily indicated and the intended use of the dielectric spacer structure can be achieved by the invention by Fu et al, Gardner et al and Wolf.

On claim 8: said silicon nitride barrier layer in Fu et al has a thickness of 2 nm – 5 nm in both the second and third embodiments ([0065] and [0067]), which substantially overlaps with the claimed range of 1.5 – 3 nm through the portion 2 – 3 nm. Furthermore, the thickness of the second silicon nitride layer by Fu et al corresponding as structure identically to the claimed etch stop layer as explained above is in the range from about 40 – 80 nm ([0066] and [0068]), which substantially overlaps the claimed range of 30 – 90 nm through the portion 40 – 80 nm.

A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See: In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 9: the thickness of the second silicon nitride layer in the third embodiment by Fu et al corresponding as structure identically to the claimed etch stop layer as explained above is in the range from about 40 – 80 nm ([0068]), which substantially overlaps the claimed range of 30 – 90 nm through the portion 40 – 80 nm.

A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See: In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 10: Both the third and second embodiments by Fu et al shall be discussed in this order:

(A) Third Embodiment: Fu et al teach in their third embodiment a spacer (Figures 13-16, title, abstract and sections [0067]-[0068]), comprising: a first spacer oxide layer 504 abutting a gate structure 501/502/503 of a MOSFET (insulated gate transistor with metal-oxide-semiconductor structure; (see sections [0060], [0067] and Figure 16 for "abutting"); a silicon-nitride layer 505 (section [0067]) deposited over said first spacer oxide layer. Furthermore, Fu et al disclose hydrogen (which is an ammonia precursor) to be substantially absent in said silicon nitride layer ([0067]) and said silicon nitride layer to be a barrier means ("means" not being specifically further limited through explicit definition in the Specification) against the diffusion or penetration of hydrogen into the first oxide layer or channel, i.e., the SiO_2-Si interface region within the wafer ([0067]).

(B) Second Embodiment: Fu et al teach in their second embodiment a spacer (Figures 9-12, title, abstract and sections [0065]-[0066]), comprising: a first spacer oxide layer 404 abutting a gate structure 401/402/403 of a MOSFET (insulated gate transistor with metal-oxide-semiconductor structure; (see sections [0060], [0065] and Figure 12 for "abutting"); a silicon-nitride layer 405 (section [0065]) deposited over said first spacer oxide layer. Furthermore, Fu et al disclose hydrogen (which is an ammonia precursor) to be substantially absent in said silicon nitride layer ([0065]) and said silicon nitride layer to be a barrier means ("means" not being specifically further limited through explicit definition in the Specification) against the diffusion or penetration of hydrogen into the first oxide layer or channel, i.e., the SiO_2-Si interface region within the wafer ([0065]).

Fu et al do not necessarily teach the further limitations (a) "wherein said silicon nitride layer includes barrier means to inhibit ammonium precursors (plural; being both hydrogen and nitrogen) from reaching and interacting with said first spacer layer", that is: that also nitrogen does not reach and interact with said first spacer layer; and (b) "a second spacer oxide layer formed over said silicon nitride layer".

However, it would have been obvious to include said further limitation ad (a) in view of Gardner et al, who teach in a patent on spacer silicon oxide / silicon nitride spacers on gate structures with LDD (see title, abstract and column 1, l. 8-39) a gate structure with a silicon oxide layer underneath a silicon nitride layer 24 (N.B.: 'nitrided oxide' is a narrower term of 'nitride') that is substantially free of nitrogen (col. 4, l. 15-28, Figure 12 and col. 10, l. 9-30) for the specific purpose of lowering the dielectric constant

(=permittivity) of the spacer so as to reduce the effects of fringing field and parasitic capacitance between gate and source/drain regions (col. 4, l. 19-28).

Motivation to include the teaching by Gardner et al in the invention by Fu et al thus derives from reducing the parasitic capacitance. *Combination* of the teaching by Gardner et al in this regard with the invention by Fu et al (third embodiment) is straightforward through adjustment if necessary of the thickness of the underlying original first spacer layer (i.e., its thickness prior to nitridization) or alternatively the overall exposure time to nitride-containing gas.

With regard to the further limitation ad (b) as defined above, it would have been obvious to include said further limitation ad (b) in view of Wolf who teaches the need to apply interlayer dielectric for planarization of gate/source/drain structures for the specific purpose to avoid unwanted steps in the topographic layout, CVD SiO2 being one of the simplest ways to implement said planarization (see sections 4.4.2.2, p. 208 and 4.4.3, p. 221). *Motivation* to include the teaching by Wolf in the invention by Fu et al flows at least from the avoidance of poor step coverage of metal lines (cf. Wolf, p. 201) that need to reach the source/drain regions such as LDD region 510 ([0067]) in Fu et al (Figure 16).

On claim 11: the only structural aspect of the further limitation as defined by claim 11 is the creation of a nitride barrier layer, taught by Fu et al as thin nitride barrier layer 505 ([0068]) in the third embodiment, 405 ([0066]) in the second embodiment, because whether said nitride barrier layer 505 *casu quo* 405 is formed through deposition means without nitridizing said first spacer oxide layer is a limitation on the

method of making: In reference to the claim language referring to ["formed through deposition means...without nitridizing said first spacer oxide layer"], intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See: In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

On claim 12: said barrier layer as disclosed by Fu et al in their third and second embodiments is formed from a layer of nitridized silicon, namely: silicon nitride ([0066] and [0068]).

On claim 13: said silicon nitride barrier layer in both the third and second embodiments in Fu et al has a thickness of 2 nm – 5 nm ([0065] and [0067]), which substantially overlaps with the claimed range of 1.5 – 3 nm through the portion 2 – 3 nm.

A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See: In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Furthermore, the thickness of the second silicon nitride layer in both the third and second embodiments by Fu et al corresponding as structure identically to the claimed etch stop layer as explained above is in the range from about 40 – 80 nm

([0066] and [0068]), which substantially overlaps the claimed range of 30 – 90 nm through the portion 40 – 80 nm.

A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See: In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 14: said barrier means block diffusion of ammonia precursors into said first spacer oxide layer, because as discussed in the rejection of claim 10 said barrier means in the invention as essentially taught by Fu et al and Gardner et al prevents the penetration of both nitrogen and hydrogen into a remaining silicon oxide layer and interface region between said silicon oxide layer (first oxide spacer layer) and the wafer.

On claim 15:

Both the third and second embodiments shall be discussed in this order:

(A) Third embodiment: Fu et al teach (third embodiment, Figures 13-16) teach a spacer stack, comprising:

a first oxide spacer layer 504 that abuts a MOSFET gate electrode 502 ([0067]);

a silicon nitride layer 506 formed over said dielectric layer ([0068]).

Fu et al do not necessarily teach the further limitation that a second oxide layer be formed over said silicon nitride layer. *However, it would have been obvious* to include said further limitation in view of Wolf who teaches the need to apply interlayer dielectric for planarization of gate/source/drain structures for the specific purpose to

avoid unwanted steps in the topographic layout, CVD SiO2 being one of the simplest ways to implement said planarization (see sections 4.4.2.2, p. 208 and 4.4.3, p. 221). *Motivation* to include the teaching by Wolf in the invention by Fu flows at least from the avoidance of poor step coverage of metal lines (cf. Wolf, p. 201) that need to reach the source/drain regions such as 510 ([0067]) in Fu et al (Figure 16). *Combination* of said teaching by Wolf with said invention is straightforward through the standard step of planarization using an oxide layer is discussed by Wolf in the above reference (p.201-208).

(B) Second embodiment: Fu et al teach (second embodiment, Figures 9-12) teach a spacer stack, comprising:

a first oxide spacer layer 404 that abuts a MOSFET gate electrode 402 ([0065]);

a silicon nitride layer 406 formed over said dielectric layer ([0066]).

Fu et al do not necessarily teach the further limitation that a second oxide layer be formed over said silicon nitride layer. *However, it would have been obvious* to include said further limitation in view of Wolf who teaches the need to apply interlayer dielectric for planarization of gate/source/drain structures for the specific purpose to avoid unwanted steps in the topographic layout, CVD SiO2 being one of the simplest ways to implement said planarization (see sections 4.4.2.2, p. 208 and 4.4.3, p. 221). *Motivation* to include the teaching by Wolf in the invention by Fu flows at least from the avoidance of poor step coverage of metal lines (cf. Wolf, p. 201) that need to reach the source/drain regions such as 410 ([0065]) or 510 ([0067]) in Fu et al (Figures 12 and 16). *Combination* of said teaching by Wolf with said invention is straightforward through

the standard step of planarization using an oxide layer is discussed by Wolf in the above reference (p.201-208).

On claim 16: said spacer structure by Fu et al further includes a barrier layer (505 in the third embodiment and 405 in the second embodiment), formed between said silicon nitride layer (506 in the third embodiment and 406 in the second embodiment) and said first oxide spacer layer (504 in the third embodiment and 404 in the second embodiment) ([0066] and [0068]).

On claim 17: said barrier layer (505 or 405 in third and second embodiments) is formed of silicon nitride having a thickness of 2 nm – 5 nm ([0067] for third embodiment, [0065] for second embodiment), which substantially overlaps the claimed range through the portion 2 – 3 nm, which at least implies *prima facie* obviousness.

A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See: In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

On claim 18: at least said barrier layer of the third embodiment 505 is formed through atomic layer deposition (Figure 14 and [0067]).

On claim 19: At least said barrier layer 405 in the second embodiment is made of silicon nitride and is formed through vapor deposition, in particular: low pressure chemical vapor deposition (LPCVD) of silicon nitride ([0065]-[0066]).

On claim 20: said barrier layer (either 405 of the second embodiment or 505 of the third embodiment) is a silicon nitride layer ([0065] and [0067]). This is the only structural limitation of the claim language of claim 20. In reference to the claim language referring to ["formed through nitridization of a silicon layer that is deposited between said silicon nitride layer and said first spacer oxide layer"], intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See: In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
October 18, 2004

Patent Examiner:

Johannes Mondt (Art Unit: 2826)